Amendments to the Specification:

Please replace paragraph [0022] beginning at page 12, line 20 with the following amended paragraphs:

-- How the offset that appears in the detection signal due to a change in temperature is eliminated will be described in detail below. To eliminate the above-mentioned offset ΔV, in a case where the resistance value of the variable resistor R2 changes from R2 to R2 $\pm$ ΔR2, the offset ΔV and the change in the resistance value of the variable resistor R2 need to fulfill the relationship expressed by formula (2) below. Suppose here that the output of the A/D conversion circuit 14 is an n-bit digital signal, the quantization unit Δv of the output value V of the A/D conversion circuit 14 equals ~~Vc / 2n~~ $Vc / 2^n$, and the outputted digital signal has a value in the range from zero to ~~2n – 1~~ 2^{n-1}. Moreover, when the output of the differential amplifier circuit A1 equals Vc / 2, the value of the digital signal outputted from the A/D conversion circuit 14 equals ~~2n – 1~~ 2^{n-1}. In this state, the offset ΔV that appears in the output value V of the A/D conversion circuit 14 due to a change in the internal resistance of the motor coil L is expressed by formula (3) below. Here, the symbol X represents an integer that fulfills ~~1 ≤X ≤2n – 1~~ $1 \leq X \leq 2^{n-1}$.--

Please replace paragraph [0023] beginning at page 13, line 10 with the following amended paragraphs:

-- $$\Delta V = A \times Io \times (\Delta R2 / R1) \times Rs \quad (2)$$

$$\Delta V = \Delta v \times X \quad (3)$$

Moreover, suppose that the variable resistor R2 changes in increments of Δr2, and that the change ΔR2 equals X $\times$ Δr2, then the relationship between Δr2 and Δv is expressed by formula (4) below. Thus, the resistance value of the variable resistor R2 is divided into n bits, with the quantization unit equal to Δr2. Here, as shown in Fig. 3, the variable resistor R2 is composed of: resistors Ra1, Ra2, . . . , Ran–1, and Ran that are

connected in series and that have resistance values ~~Δr2 × 2n 1, Δr2 × 2n 2, . . . , Δr2 × 21, and Δr2 × 20~~ $\Delta r2 \times 2^{n-1}$, $\Delta r2 \times 2^{n-2}$, . . . , $\Delta r2 \times 2^{1}$, and $\Delta r2 \times 2^{0}$, respectively; and MOS transistors T1 to Tn that are connected in parallel with the resistors Ra1 to Ran, respectively. That is, the resistance value R2 of the variable resistor R2 can be varied within the range of ~~0 ≤R2 ≤Δr2 × 2n 1~~ $0 \leq R2 \leq \Delta r2 \times 2^{n-1}$.--

Please replace paragraph [0024] beginning at page 14, line 1 with the following amended paragraphs:

-- $\Delta v = A \times Io \times (\Delta r2 / R1) \times Rs$ (4)

Let the middle value of the resistance value of the variable resistor ~~R2 be Rx (=Δr2 × 2n 1)~~ R2 be Rx ($=\Delta r2 \times 2^{n-1}$), then the resistance values of the resistors ~~Ra1, Ra2, . . . , Ran 1, and Ran equal Rx / 20, Rx / 21, . . . , Rx / 2n 2, and Rx / 2n 1~~ Ra1, Ra2, . . . , Ran−1, and Ran equal $Rx / 2^{0}$, $Rx / 2^{1}$, . . . , $Rx / 2^{n-2}$, and $Rx / 2^{n-1}$, respectively. The relationship between this resistance value Rx and the direct-current voltage Vc is expressed by formula (5) below. Thus, the current value Io may be constant, in which case the resistance value Rx equals $Vc \times R1 / (2 \times A \times Io \times Rs)$, or alternatively the resistance value RX may be constant, in which case the current value Io equals $Vc \times R1 / (2 \times A \times Rx \times Rs)$.--

Please replace paragraph [0030] beginning at page 16, line 20 with the following amended paragraphs:

-- The initial setting operation of the back electromotive force detection circuit 12 configured as described above will be described below with reference to the timing charts shown in Figs. 5 and 6. Here, it is assumed that n = 4, and thus that the A/D conversion circuit 14 performs conversion into a four-bit digital signal. Specifically, the variable resistor R2 is composed of resistors Ra1, Ra2, Ra3, and Ra4 having resistance values ~~Rx~~

~~/ 20, Rx / 21, Rx / 22, and Rx / 23~~ Rx / 2^0, Rx / 2^1, Rx / 2^2, and Rx / 2^3, respectively, and MOS transistors T1 to T4 connected in parallel with the resistors Ra1 to Ra4, respectively.--

Please replace paragraph [0031] beginning at page 17, line 4 with the following amended paragraphs:

-- At the start of the initial setting operation, in response to a signal corresponding to ~~(24 – 1)10 = (1000)2~~ $(2^4 - 1)_{10} = (1000)_2$, the MOS transistor T1, which receives at its gate a signal corresponding to "1" in the first digit from the offset calculation circuit 15 is turned off, and the MOS transistors T2 to T4, which receive at their gates signals corresponding to "0" in the second to fourth digits, are turned on. As a result, in the variable resistor R2, the Ra1 and the MOS transistors T2 to T4, which are turned on, are connected in series, and thus the variable resistor R2 has a resistance value ~~Rx / 20~~ Rx / 2^0.--

Please replace paragraph [0032] beginning at page 17, line 12 with the following amended paragraphs:

-- Subsequently, when the offset is checked with the magnetic head 21 kept in contact with the spindle 23, as shown in Fig. 5, when the first internal clock pulse C1 is inputted to the back electromotive force detection circuit 12, the drive current fed to the motor coil L is made equal to zero. Then, when the second internal clock pulse C2 is inputted, the offset calculation circuit 15 reads the output X1 from the A/D conversion circuit 14, and stores ~~(X1 – 8)10~~ $(X1 - 8)_{10}$ as the offset to be fed to the subtraction circuit 16.--

Please replace paragraph [0033] beginning at page 17, line 19 with the following amended paragraphs:

-- Subsequently, as shown in Fig. 5, when the third internal clock pulse C3 is inputted, the current value of the drive current fed to the motor coil L is made equal to Io, which has a positive value. Thereafter, when the fourth internal clock pulse C4 is inputted, the output X2 from the A/D conversion circuit 14 is read to calculate ~~(8 – (X2 – X1))10~~ $(8 - (X2 - X1))_{10}$, and a four-bit signal corresponding to ~~(8 – (X2 – X1))10~~ $(8 - (X2 - X1))_{10}$ is outputted to the variable resistor R2. Thus, with the four-bit signal corresponding to ~~(8 – (X2 – X1))10~~ $(8 - (X2 - X1))_{10}$, the MOS transistors T1 to T4 are turned on or off, and the resistance value of the variable resistor R2 is set accordingly.--

Please replace paragraph [0034] beginning at page 18, line 4 with the following amended paragraphs:

-- For example, suppose that the output X1 read when the internal clock pulse C2 is fed in is ~~(1001)2~~ $(1001)_2$, and that the output X2 read when the internal clock pulse C4 is fed in is ~~(1011)2~~ $(1011)_2$. In this case, when the internal clock pulse C2 is fed in, as the offset to be fed to the subtraction circuit ~~16, (X1 – 8)10 = (0001)2~~ 16, $(X1 - 8)_{10} = (0001)_2$ is stored in the offset calculation circuit 15.--

Please replace paragraph [0035] beginning at page 18, line 9 with the following amended paragraphs:

-- Later, when the internal clock pulse C4 is fed in, ~~(8 – (X2 – X1))10 = (1000 – (1011 – 1001))2 = (0110)2~~ $(8 - (X2 - X1))_{10} = (1000 - (1011 - 1001))_2 = (0110)_2$ is calculated by the offset calculation circuit 15, and is fed to the variable resistor R2. Thus,

the MOS transistors T2 and T3, which receive at their gates signals corresponding to "1" in the second and third digits, are turned off, and the MOS transistors T1 and T4, which receive at their gates signals corresponding to "0" in the first and fourth digits, are turned on. As a result, in the variable resistor R2, the resistors Ra2 and Ra3 and the MOS transistors T1 and T4, which are turned on, are connected in series, and thus the resistance value of the variable resistor ~~R2 now equals Rx / 21 + Rx / 22~~ R2 now equals $Rx / 2^1 + Rx / 2^2$.--

Please replace paragraph [0036] beginning at page 18, line 19 with the following amended paragraphs:

-- Suppose now that the output X1 read when the internal clock pulse C2 is fed in is ~~(1001)2~~ $(1001)_2$, and that the output X2 read when the internal clock pulse C4 is fed in is ~~(0111)2~~ $(0111)_2$. In this case, when the internal clock pulse C2 is fed in, as the offset to be fed to the subtraction circuit ~~16, (X1 – 8)10 = (0001)2~~ 16, $(X1 - 8)_{10} = (0001)_2$ is stored in the offset calculation circuit 15.--

Please replace paragraph [0037] beginning at page 18, line 24 with the following amended paragraphs:

-- Later, when the internal clock pulse C4 is fed in, ~~(8 – (X2 – X1))10 = (1000 – (0111 – 1001))2 = (1010)2~~ $(8 - (X2 - X1))_{10} = (1000 - (0111 - 1001))_2 = (1010)_2$ is calculated by the offset calculation circuit 15, and is fed to the variable resistor R2. Thus, the MOS transistors T1 and T3, which receive at their gates signals corresponding to "1" in the first and third digits, are turned off, and the MOS transistors T2 and T4, which receive at their gates signals corresponding to "0" in the second and fourth digits, are turned on. As a result, in the variable resistor R2, the resistors Ra1 and Ra3 and the MOS transistors T2 and T4, which are turned on, are connected in series, and thus the

resistance value of the variable resistor ~~R2 now equals Rx / 20 + Rx / 22~~ R2 now equals $Rx / 2^0 + Rx / 2^2$.--

Please replace paragraph [0038] beginning at page 19, line 10 with the following amended paragraphs:

-- On the other hand, when the offset is checked with the magnetic head 21 kept in contact with the ramp area 22, as shown in Fig. 6, when the first internal clock pulse C1 is inputted to the back electromotive force detection circuit 12, the drive current fed to the motor coil L is made equal to zero. Then, when the second internal clock pulse C2 is inputted, the offset calculation circuit 15 reads the output X1 from the A/D conversion circuit 14, and stores ~~(X1 – 8)10~~ $(X1 - 8)_{10}$ as the offset to be fed to the subtraction circuit 16.--

Please replace paragraph [0039] beginning at page 19, line 17 with the following amended paragraphs:

-- Subsequently, as shown in Fig. 6, when the third internal clock pulse C3 is inputted, the current value of the drive current fed to the motor coil L is made equal to –Io, which has a negative value. Thereafter, when the fourth internal clock pulse C4 is inputted, the output X2 from the A/D conversion circuit 14 is read to calculate ~~(8 + (X2 – X1))10~~ $(8 + (X2 - X1))_{10}$, and a four-bit signal corresponding to ~~(8 + (X2 – X1))10~~ $(8 + (X2 - X1))_{10}$ is outputted to the variable resistor R2. Thus, with the four-bit signal corresponding to ~~(8 + (X2 – X1))10~~ $(8 + (X2 - X1))_{10}$, the MOS transistors T1 to T4 are turned on or off, and the resistance value of the variable resistor R2 is set accordingly.--

Please replace paragraph [0040] beginning at page 20, line 2 with the following amended paragraphs:

-- For example, suppose that the output X1 read when the internal clock pulse C2 is fed in is ~~(1001)2~~ $(1001)_2$, and that the output X2 read when the internal clock pulse C4 is fed in is ~~(1011)2~~ $(1011)_2$. In this case, when the internal clock pulse C2 is fed in, as the offset to be fed to the subtraction circuit ~~16, (X1 – 8)10 = (0001)2~~ 16, $(X1 - 8)_{10} = (0001)_2$ is stored in the offset calculation circuit 15.--

Please replace paragraph [0041] beginning at page 20, line 7 with the following amended paragraphs:

-- Later, when the internal clock pulse C4 is fed in, ~~(8 + (X2 – X1))10 = (1000 + (1011 – 1001))2 = (1010)2~~ $(8 + (X2 - X1))_{10} = (1000 + (1011 - 1001))_2 = (1010)_2$ is calculated by the offset calculation circuit 15, and is fed to the variable resistor R2. Thus, the MOS transistors T1 and T3, which receive at their gates signals corresponding to "1" in the first and third digits, are turned off, and the MOS transistors T2 and T4, which receive at their gates signals corresponding to "0" in the second and fourth digits, are turned on. As a result, in the variable resistor R2, the resistors Ra1 and Ra3 and the MOS transistors T2 and T4, which are turned on, are connected in series, and thus the resistance value of the variable resistor ~~R2 now equals Rx / 20 + Rx / 22~~ R2 now equals $Rx / 2^0 + Rx / 2^2$.--

Please replace paragraph [0042] beginning at page 20, line 17 with the following amended paragraphs:

-- Suppose now that the output X1 read when the internal clock pulse C2 is fed in is ~~(1001)2~~ $(1001)_2$, and that the output X2 read when the internal clock pulse C4 is fed in is ~~(0111)2~~ $(0111)_2$. In this case, when the internal clock pulse C2 is fed in, as the offset to

be fed to the subtraction circuit ~~16, (X1 8)10 = (0001)2~~ 16, $(X1 - 8)_{10} = (0001)_2$ is stored in the offset calculation circuit 15.--

Please replace paragraph [0043] beginning at page 20, line 22 with the following amended paragraphs:

-- Later, when the internal clock pulse C4 is fed in, ~~(8 + (X2 X1))10 = (1000 + (0111 1001))2 = (0110)2~~ $(8 + (X2 - X1))_{10} = (1000 + (0111 - 1001))_2 = (0110)_2$ is calculated by the offset calculation circuit 15, and is fed to the variable resistor R2. Thus, the MOS transistors T2 and T3, which receive at their gates signals corresponding to "1" in the second and third digits, are turned off, and the MOS transistors T1 and T4, which receive at their gates signals corresponding to "0" in the first and fourth digits, are turned on. As a result, in the variable resistor R2, the resistors Ra2 and Ra3 and the MOS transistors T1 and T4, which are turned on, are connected in series, and thus the resistance value of the variable resistor ~~R2 now equals Rx / 21 + Rx / 22~~ R2 now equals $Rx / 2^1 + Rx / 2^2$.--

Please replace paragraph [0044] beginning at page 21, line 8 with the following amended paragraphs:

-- Through operations as performed in the different examples described above, the value obtained by eliminating from the output of the differential amplifier circuit A2 the offset due to the internal resistance of the motor coil L is outputted from the A/D conversion circuit 14. Thus, when the internal clock pulse C5 is fed in with the current value of the drive current to the motor coil L kept equal to Io, which has a positive value, the output from the A/D conversion circuit 14 equals ~~(1001)2~~ $(1001)_2$. Then, the subtraction circuit 16 subtracts the offset ~~(0001)2~~ $(0001)_2$, and thus the detection signal outputted from the subtraction circuit 16 has a value ~~(1000)2~~ $(1000)_2$.--